Introduction to Digital Logic

EECS/CSE 31L

**Final Assignment Design Report**

**Designing a Processor**

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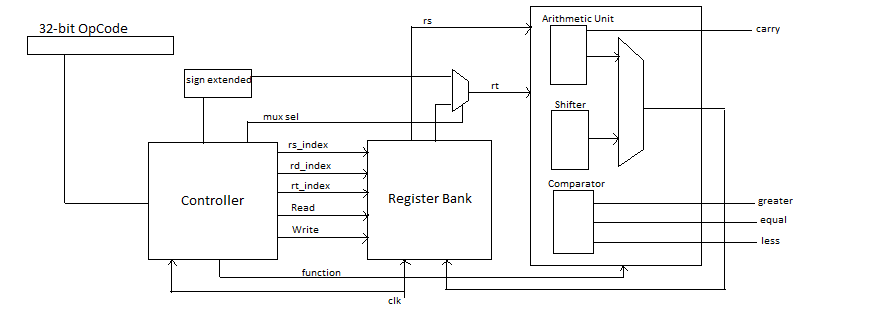
1 BLOCK Description

This 32-bit processor is designed to accept a 32-bit instructional code and performs a series of operations depending on the information of the instruction. The instruction code is divided into 6 parts. The first bit is the bit that determines whether an immediate value or another target register will be used to perform the specified operation. The next 6 bits determine the source register address being used as the first operand of the code. The next 6 bits determine the destination register address where the result will be stored in the register. The next 4 bits is the opcode for the entire system. There are 15 opcode choices from 0000 to 1011. The next 6 bits determine the second register being used in the operation. Depending on whether the first bit is 1 or 0, the second register can be combined with the next 9 bit immediate value to become a 15 bit immediate value that will be used with the source register. If the first bit is 0 then the remaining last 9 bits of the code will just be immediate values.

2 Input/Output Port Description

|  |  |  |  |
| --- | --- | --- | --- |
| Port Name | Port Type | Port Size | Description |
| clk | IN | 1 | Clock signal for the circuit |
| inst | IN | 32 | The 32-bit instruction code, the Opcode |
| great | OUT | 1 | Signal if the first number is greater than the other |
| less | OUT | 1 | Signal if the first number is less than the other |
| equal | OUT | 1 | Signal if both the first and other number are equal |
| carry | OUT | 1 | The carry out bit |
| over\_flow | OUT | 1 | Signal for overflow in calculations |

3 Design Schematic



4 Waveforms

